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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/598,054 | 06/18/2007 | Jurgen Fischer | E0196.0105 | 9614 |

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| EXAMINER | |
|---|---|
| SODERHOLM, KRISTA Z | |
| ART UNIT | PAPER NUMBER |
| 2826 | |
| MAIL DATE | DELIVERY MODE |
| 09/29/2008 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/598,054 | FISCHER ET AL. | |
| | Examiner | Art Unit | |
| | KRISTA SODERHOLM | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *6-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 August 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/29/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, integrated circuit formed on the one side of the substrate must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 6, 19-21, 22 and 25-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Endroes (5,650,363).

3. Regarding claim 6, Endroes teaches an integrated circuit arrangement comprising, a non-planar substrate 2, on which an integrated circuit 1 is placed wherein the side where the integrated circuit is placed is arranged on a carrier 4 that is produced from a chemically resistant material (glass).

4. Regarding claim 19, Endroes teaches that the entire area of the side of the substrate is connected to the carrier (see fig 3).

5. Regarding claim 20, Endroes teaches that the carrier has a cavity where the substrate is completely held (see fig 3).

6. Regarding claim 21, Endroes teaches that the carrier has a cavity where the substrate is completely held (see fig 3).

7. Regarding claim 22, Endroes teaches an integrated circuit arrangement comprising, a curved substrate 2, having an integrated circuit 1 is placed on the outer surface of and the outer surface of the substrate is arranged on a carrier 4 that is produced from a chemically resistant material (glass).

8. Regarding claim 25, Endroes teaches that the carrier has a cavity where the entire area of the outerside of the substrate is connected to the carrier (see fig 3).

9. Regarding claim 26, Endroes teaches that the carrier has a cavity where the curved substrate is completely held (see fig 3).

***Claim Rejections - 35 USC § 103***

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 7, 12-14 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endroes (5,650,363) in view of Bourdelaise (5,027,191).

12. Regarding claim 7, Endroes teaches the limitations of claim 6 above, but fails to teach that the carrier is comprised of ceramic. Bourdelaise teaches a chip carrier that is comprised of a ceramic material, to provide for a hermetic isolation of the chip from the outside environment. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the ceramic carrier of Bourdelaise with the package of Endroes to hermetically seal the chip from the outside environments.

13. Regarding claim 12, Endroes teaches that the entire area of the side of the substrate is connected to the carrier (see fig 3).

14. Regarding claim 13, Endroes teaches that the carrier has a cavity where the substrate is completely held (see fig 3).

15. Regarding claim 14, Endroes teaches that the carrier has a cavity where the substrate is completely held (see fig 3).

16. Regarding claim 23, Endroes teaches the limitations of claim 22 above, but fails to teach that the carrier is comprised of ceramic. Bourdelaise teaches a chip carrier that is comprised of a ceramic material, to provide for a hermetic isolation of the chip from the outside environment. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the ceramic carrier of Bourdelaise with the package of Endroes to hermetically seal the chip from the outside environments.

17. Claims 15-18 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endroes (5,650,363) in view of Rissing (2005/0098472).

18. Regarding claim 15, Endroes teaches the limitations of claim 6 above, but fails to teach that a side of the carrier away from the integrated circuit has a planar surface. Rising teaches a chip carrier 1 with a planar surface 4 away from the integrated circuit that has a planar surface to hold a cover element 6. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the planar surface of Rissing with the arrangement of Endroes to securely hold a cover element.

19. Regarding claim 16, Endroes teaches that the entire area of the side of the substrate is connected to the carrier (see fig 3).

20. Regarding claim 17, Endroes teaches that the carrier has a cavity where the substrate is completely held (see fig 3).

21. Regarding claim 18, Endroes teaches that the carrier has a cavity where the substrate is completely held (see fig 3).

22. Regarding claim 24, Endroes teaches the limitations of claim 22 above, but fails to teach that a side of the carrier away from the integrated circuit has a planar surface. Rising teaches a chip carrier 1 with a planar surface 4 away from the integrated circuit that has a planar surface to hold a cover element 6. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the planar surface of Rissing with the arrangement of Endroes to securely hold a cover element.

23. Claims 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endroes (5,650,363) in view of Bourdelaise (5,027,191) as applied to claim 7 above, and further in view of Rissing (2005/0098472).

24. Regarding claim 8, Endroes in view of Bourdelaise teaches the limitations of claim 7 above but fails to explicitly teach that a side of the carrier away from the integrated circuit has a planar surface. Rising teaches a chip carrier 1 with a planar surface 4 away from the integrated circuit that has a planar surface to hold a cover element 6. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the planar surface of Rissing with the arrangement of Endroes in view of Bourdelaise to securely hold a cover element.

25. Regarding claim 9, Endroes teaches that the entire area of the side of the substrate is connected to the carrier (see fig 3).

26. Regarding claim 10, Endroes teaches that the carrier has a cavity where the substrate is completely held (see fig 3).

27. Regarding claim 11, Endroes teaches that the carrier has a cavity where the substrate is completely held (see fig 3).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KRISTA SODERHOLM whose telephone number is (571)272-8344. The examiner can normally be reached on M and Th 6:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leonardo Andújar/
Primary Examiner, Art Unit 2826

/KZS/